SPECIFICATION

THIN FILM TRANSISTOR AND METHOD OF MANUFACTURING THE SAME AND DISPLAY APPARATUS USING THE TRANSISTOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a thin film transistor (TFT), and particularly to a thin film transistor used in a display device.

2. Description of Related Art

[0002] A conventional TFT disclosed by U.S. Pat. No. 5,349,205 is shown in FIG. 14. The TFT 100 comprises a substrate 10, a gate electrode 20 formed on the substrate 10, a gate protection layer 30 covering the gate electrode 20, a gate insulation layer 40 arranged on the substrate 10 and the gate protection layer 30, an amorphous silicon layer 50 formed on the gate insulation layer 40, two phosphor-doped amorphous silicon layers 60a and 60b arranged on the two sides of the amorphous silicon layer 50, a source electrode 70a formed on the phosphor-doped amorphous silicon layer 60a and the gate insulation layer 40, and a drain electrode 70b formed on the phosphor-doped amorphous silicon layer 60b and the gate insulation layer 40.

[0003] The cross-section of the gate electrode 20 is in a shape of rectangle. Each of the gate insulation layer 40, the amorphous silicon layer 50 has two opposite incline surfaces. Each of the two phosphor-doped amorphous silicon layers 60a, 60b, the source electrode 70a, and the drain electrode 70b has an incline

surface.

[0004] These incline surfaces are produced in the process of deposit, spray or plating. But, a flat surface is better for attaining a good character of coating. So we do my best to flatten the incline surfaces.

[0005] In a closed circuit composed of resistance and a capacitance, a RC delay is produced, which delay the signal transmission therein. For lowering the RC delay, methods can be used as follows: Firstly, using a low impedance material to make the gate electrode 20, such as Al, Cr, Ta, its alloy, and so on; Secondly, increasing the thickness and width of the gate electrode 20 to enlarge its cross-section area. Increasing the width of the gate electrode 20 reduces the aperture ratio of the liquid crystal display, which lowers the light output efficiency. Furthermore, increasing the thickness of the gate electrode 20 makes the incline surface steeper and lowers the character of coating.

SUMMARY OF THE INVENTION

[0006] An object of the present invention is to reduce an RC delay of a scanning signal in a TFT.

[0007] In order to achieve the object set forth, a TFT includes a substrate, a gate electrode disposed in the substrate, a gate insulation layer disposed on the substrate and gate electrode, a channel layer disposed on the gate insulation layer, a source ohmic contact layer and a drain ohmic contact layer arranged on the channel layer and at the end of the channel layer, a source electrode disposed on the substrate and source ohmic contact layer, a drain electrode disposed on the substrate and drain ohmic contact layer.

[0008] Because of the gate electrode disposed in the substrate, it is easy to increase the thickness of the gate electrode. In other words, it is easy to reduce the resistance of the gate electrode. So the present invention can overcome the above described disadvantage.

[0009] Other objects, advantages and novel features of the invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a cross-section view of a TFT according to the present invention;

[0011] FIG. 2 is a diagrammatic view of a display device using the TFT as shown in FIG. 1;

[0012] FIG. 3 is a cross-section view of the display device as shown in FIG. 2;

[0013] FIG. 4 to FIG. 9 indicate the processes of producing a gate electrode of the TFT as shown in FIG. 1;

[0014] FIG. 10 to FIG. 13 indicate the latter processes of manufacturing the TFT as shown in FIG. 1; and

[0015] FIG. 14 is a cross-section view of a conventional TFT.

DETAILED DESCRIPTION OF THE INVENTION

[0016] Referring to FIG. 1, there is a cross-section view of a TFT according to a first embodiment of the present invention. The TFT 200 includes a substrate

1, a gate electrode 2 disposed in the substrate 1, a gate insulation layer 4 disposed on the substrate 1 and the gate electrode 2, a channel layer 5 disposed on the gate insulation layer 4, a source ohmic contact layer 6a and a drain ohmic contact layer 6b arranged on two ends of the channel layer 5 respectively, a source electrode 7a disposed on the substrate 1 and the source ohmic contact layer 6a, a drain electrode 7b disposed on the substrate 1 and drain ohmic contact layer 6b.

[0017] The surface of the gate electrode 2 is parallel with the surface of the substrate 1. The substrate 1 can be made from glass or silicon oxide. The material of the gate electrode 2 can be metal conductive material, such as, Cu, Al, Ti, Mo, Cr, Nd, Ta, or its alloy, and so on. The gate insulation layer 4 can be made of silicon nitride or silicon oxide. The channel layer 5 can use amorphous silicon or polycrystalline silicon. The ohmic contact layer 6a and 6b can adopt amorphous silicon or phosphor-doped polycrystalline silicon. The surface of the gate electrode 2 is parallel with the surface of the substrate.

[0018] Referring to FIG. 2, there is a diagrammatic view of a display device using the TFT 100 according to a second embodiment of the present invention. The gate electrode 2 is contacted with a scanning line 17, and the source electrode 7a is contacted with a signal line 18, and the drain electrode 7b is contacted with a pixel electrode 11. The gate electrode 2 receives a signal transported by the scanning line 17. A signal transported by the signal line 18 is received by the source electrode 7a, and then output by the drain electrode 7b to the pixel electrode 11. The pixel electrode 11 holds the potential depending on a storage capacitance (not shown) until the gate electrode 2 next operation.

[0019] Referring to FIG. 3, there is a cross-section view of a display device as

shown in FIG. 2. A protection layer 19 is formed on the thin film transistor. The pixel electrode 11 is formed on the protection layer 19 and drain electrode 7b. The storage capacitance comprises the pixel electrode 11, the gate insulation layer 4, the protection layer 19, and the scanning line 17. A color filter 14 and a black matrix 15 are formed on a substrate 16. A common electrode 13 is formed on the color filter 14 and the black matrix 15. A liquid crystal layer 12 is arranged between the pixel electrode 11 and the common electrode 13. The display device is driven by the TFT, so the display efficiency is decided by the potential of the pixel electrode 11.

[0020] Because of the gate electrode 2 is deposited in the substrate 1, the thickness of the gate electrode 2 can be changed with the depth of the substrate 1 etched. Thus it is easy to increase the thickness of the gate electrode 2 to reduce the its impedance. Furthermore, the height of the gate electrode 2 can almost be equal to that of the substrate. Therefore, the TFT 100 can efficiently reduce a RC delay of a scanning signal.

[0021] A method of producing the thin film transistor as shown in FIG. 1 comprises: a photo mask process of producing the gate electrode 2, and a latter processes of manufacturing the thin film transistor.

[0022] The photo mask processes of producing the gate electrode 2 shown in FIG. 4 to FIG. 9 have steps as follows:

Firstly, as shown in FIG. 4, coating a photo-resist film 8 on a substrate 1, and baking the photo-resist film 8;

Secondly, as shown in FIG. 5, using an ultraviolet light to expose the photo-resist film 8 through a photo mask having a predetermined pattern by

projection manner, and then forming a pattern by developing;

Thirdly, as shown in FIG. 6, forming a slot 2a on the substrate 1 by method of dry etching or wet etching;

Fourthly, as shown in FIG. 7, wiping off the residual of the photo-resist film 8 by a method of dissolving, oxidizing, or directly peeling off;

And then, as shown in FIG. 8, depositing a metal layer 3 on the substrate 1 to fill the slot 2a;

Lastly, as shown in FIG. 9 , wiping off the metal on the substrate 1 by polishing to form a gate electrode 2, and the gate electrode 2 fills the slot 2a.

[0023] Some changes can be made in the former process of producing the gate electrode 2. Such as:

omitting the step of wiping off the residual of the photo-resist film 8 as shown in FIG. 7, directly depositing the metal layer 3 on the substrate 1 and the photo-resist film 8, and then wiping off the photo resist film 8 to form the gate electrode 2;

the photo-resist film 8 formed on the metal layer 3, using an ultraviolet light to expose the photo-resist film 8 through a photo mask having a predetermined pattern by projection manner, and then forming a pattern by developing, wiping off the metal around the slot 2a and the photo-resist film 8 to form the gate electrode 2.

[0024] The latter processes of producing the thin film transistor is shown in FIG. 10 to FIG. 13 and FIG. 1.

[0025] First, shown as FIG. 10, using chemical vapor deposition (CVD) to forming the gate insulation layer 4, wherein the reaction gases are silicon alkyl and ammonia. And then using a method of CVD to forming an amorphous silicon

layer 9 on the insulation layer 4, wherein the reaction gases are silicon chloride and hydrogen. After that, forming a phosphor doped amorphous silicon layer 6 on the amorphous silicon layer 9 by doping technology.

[0026] Second, shown as FIG. 11, using photo mask process to etch two sides of the amorphous silicon layer 9 and the phosphor doped amorphous silicon layer 6 till showing up the gate insulation layer 4. **[0027]** Third, shown as FIG. 12, depositing a source and drain metal layer 7 on the phosphor amorphous layer 6 and the gate insulation layer 4.

[0028] Subsequently, shown as FIG. 13, using photo mask process to etch the middle area of the source and drain metal layer 7 till showing up the amorphous silicon layer 6, and then forming a source electrode 7a and a drain electrode 7b.

[0029] Last, wiping off the middle area of the phosphor doped amorphous silicon layer 6 by a method of dry etching, and then forming a gate ohmic contact layer 6a, a drain ohmic contact layer 6b and a channel layer 5. That is, the TFT 100 as shown in FIG. 1 is produced.

[0030] And the section shape of the gate electrode 2 is not only trapezoid, further, its section shape is also rectangle.

[0031] It is to be understood, however, that even though numerous characteristics and advantages of the present invention have been set forth in the foregoing description, together with details of the structure and function of the invention, the disclosure is illustrative only, and changes may be made in detail, especially in matters of shape, size, and arrangement of parts within the principles of the invention to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed.